AMENDMENT

In the Claims:

Please amend claims 1 and 38, as follows:

1. (Currently Amended) An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer that comprises ~~metal~~ aluminum regions disposed between dielectric regions;

a protective overcoat formed over the metallization layers and having vias through it, wherein the protective overcoat comprises one or more layers selected from a group consisting of a silicon oxynitride layer, a silicon oxide layer, and a silicon nitride layer;

a conductive barrier layer conformal to the vias, a bottom surface of the conductive barrier layer abutting at least one of the aluminum regions;

tungsten plugs substantially filling the vias ~~and connecting to one of the metal regions in the uppermost layer~~; and

thick copper formed over the protective overcoat and forming connections to the tungsten plugs.

2. (Cancelled).

3. (Cancelled).

4. (Cancelled).

5. (Cancelled).

6. (Cancelled).

7. (Original) The integrated circuit of claim 1, wherein the thick copper forms interconnections between device elements within the integrated circuit.

8. (Cancelled)

9. (Cancelled).

10. (Cancelled).

11. (Cancelled).

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Cancelled).

16. (Previously Presented) An integrated circuit, comprising:

a semiconductor substrate comprising device elements and one or more metallization layers interconnecting the device elements, the one or more metallization layers having an uppermost layer, the uppermost layer comprising bond pads;

a protective overcoat formed over the metal layers and having vias through it, wherein multiple vias are formed over individual bond pads respectively, and wherein the protective overcoat comprising one or more layers selected from the group consisting of a silicon oxynitride layer, a silicon oxide layer, and a silicon nitride layer;

metal plugs substantially filling the vias and connecting to the bond pads; and

thick copper connections to the metal plugs.

17. (Original) The integrated circuit of claim 16, wherein the metal plugs are copper plugs.

18. (Cancelled).

19. (Original) The integrated circuit of claim 16, wherein the metal plugs have a coefficient of thermal expansion less than or equal to about 8 ppm/°C.

20. (Original) The integrated circuit of claim 16, wherein the metal plugs are tungsten plugs.

21. (Original) The integrated circuit of claim 16, wherein the uppermost layer is an aluminum metallization layer.

22. (Cancelled).

23. (Original) The integrated circuit of claim 16, wherein the thick copper connections comprise interconnections between device elements within the integrated circuit.

24. (Cancelled)

25. (Cancelled)

26. (Cancelled).

27. (Cancelled).

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Cancelled).

33. (Previously Presented) The integrated circuit of claim 1, wherein some of the tungsten plugs couple the thick copper to one of the metal regions.

34. (Previously Presented) The integrated circuit of claim 1, wherein the thick copper substantially overlies at least one of the metal regions.

35. (Previously Presented) The integrated circuit of claim 1, wherein the thick copper does not extend over at least a portion of at least one of the dielectric regions.

36. (Previously Presented) The integrated circuit of claim 16, wherein the multiple metal plugs individually couple the thick copper connections to the bond pads.

37. (Cancellled).

38. (Currently Amended) The integrated circuit of claim 1, ~~further comprising a copper seed layer formed directly onto the surface of each of the tungsten plugs,~~ wherein the ~~copper seed layer comprises a~~ conductive barrier layer is adapted to prevent copper from diffusing into the protective overcoat.